

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (cancelled)

2. (amended) The sensor of claim [1] 25, further comprising:

a first clocking structure disposed over and transverse to the plurality of first channel structures, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode; and

a second clocking structure disposed over and transverse to the plurality of second channel structures, wherein the second clocking structure includes a transfer gate electrode and a delay well electrode.

3. (original) The sensor of claim 2, wherein:

the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure; and

the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure.

4. (amended) The sensor of claim [1] 25, wherein each pixel of each row of pixels includes at least one of a photo diode and a pinned photo diode.

5. (original) A method of using the sensor of claim 2 comprising steps of:

applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure;

applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and

applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied.

6. (amended) A line scan sensor comprising:

first and second rows of pixels defined along respective first and second lines, the first line being spaced from and parallel to the second line;

corresponding first and second readout registers;

a first clocking structure disposed between the first row of pixels and the first readout register, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode; and

a second clocking structure disposed between the second row of pixels and the second readout register, wherein the second clocking structure includes a transfer gate electrode and a delay well electrode.

7. (original) The sensor of claim 6, wherein the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure.

8. (cancelled)

9. (amended) The sensor of claim [8] 7, wherein the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure.

10. (amended) The sensor of claim [8] 6, further comprising:

a plurality of first channel structures coupled between the first row of pixels and the first readout register, each channel structure of the first channel structures being disposed under and transverse to the first clocking structure and between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and

a plurality of second channel structures coupled between the second row of pixels and the second readout register, each channel structure of the second channel structures being disposed under and transverse to the second clocking structure and between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register.

11. (amended) A method of using the sensor of claim [8] 6 comprising steps of:

applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure;

applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and

applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied.

12. (original) A method of using the sensor of claim 6 comprising steps of:

applying a transfer clock pulse to the transfer gate electrode of the first clocking structure; and

applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied.

13. (amended) The sensor of claim 6, wherein each pixel of each row of pixels includes at least one of a photo diode and a pinned photo diode.

14. (cancelled)

15. (amended) The sensor of claim [14] 6, further comprising a summation circuit to combine serial outputs from the first and second readout registers, the summation circuit being disposed on a same chip as the first and second readout registers.

16. (cancelled)

17. (amended) The sensor of claim [14] 6, wherein each pixel of the first and second row of pixels includes a storage well and at least one of a photo diode and a pinned photo diode.

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (cancelled)

24. (cancelled)

25. (new) A line scan sensor comprising:

first and second rows of pixels defined along respective first and second lines, the first line being spaced from and parallel to the second line;

corresponding first and second readout registers, an end register element of the first readout register being coupled to an end register element of the second readout register, the coupled end register elements being coupled so as to function as a single output node of a readout register;

a plurality of first channel structures, each channel structure of the first channel structures being disposed between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and

a plurality of second channel structures, each channel structure of the second channel structures being disposed between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register.